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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,861	09/26/2001	Michael Frank	ATI.0100580	1604

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EXAMINER
DINH, NGOC V

ART UNIT	PAPER NUMBER
2187	2

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,861	FRANK ET AL.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C 103(a) as being unpatentable over Chin et al [U.S 6,202,10[illegible], and in view of Kark et al [U.S 6,052,772].

1. **As per claims 1, 2-4, 8:**

Chin teaches a method comprising the steps of:

Receiving a first request to access data from a first memory device [abstract; 18, 32a, fig. 1]; preparing the first request for the data for access through the first memory device;

Providing a second request to access the data from a second memory device [16, fig. 1], wherein the second request is provided concurrently with the step of preparing the first request [col. 1, lines 9-15; col. 5, lines 35-45; col. 7, line 20 to col. 8, line 65; col. 11, lines 45-55].

Inherently, Chin teaches receiving a first notification that the data associated with the first request is available from the second memory device [16, cache, fig. 1]. This is because a request access to the cache will result a hit/miss, this causes the hit/miss notification signal inside the caches is asserted. The notification signal is sent to the memory controller to confirm that the data associated with the request is in the cache. Chin further teaches the data in the second memory is coherent with the data in the first memory [col. 3, lines 50-60]; the first memory device is a RAM [col. 2, lines 63-67]; the second memory includes cache memory [16, fig. 1].

Chin does not teach terminating the first request, in response to the first notification; terminating first request includes terminating the first request in a memory controller before the first request is sent to the first memory device; terminating first request

9. As per claims 20-22:

Chin inherently teaches bus interface unit further used to synchronize said cache memory to said memory device; bus interface unit to determine validity includes determining a coherency between said cache memory and said memory device; coherency is dependent on whether said memory device has been written to prior to a synchronization of said cache memory with said memory device. This is because there is a discrepancy between data in the cache and data in the memory device as the cache, as the cache has more up-to-date data than memory device due to the simultaneously accesses to the cache, and data in the memory device is considered stale. In order to ensure the coherency between the cache and the memory, the updated line from the cache is extracted and copied into memory device so the data in both cache and memory device is coherent. This process is called synchronization cache.

10. As per claims 23-24:

Chin teaches said bus controller includes a peripheral component interconnect bus controller [40, fig. 2]; memory device includes random access memory [col. 2, lines 63-67].

11. As per claim 25:

Implicitly, Chin teaches memory controller further used to: assign a first identifier to said first request; and 3 identify said first request from a plurality of pending requests using said first identifier [col. 3, line 65 to col. 4, line 55]. This is because when the CPU or I/O device generates a plurality of requests, each request must have its own identification so the memory controller can return requested data to appropriate request.

Claims 26 are rejected under 35 U.S.C 103(a) as being unpatentable over Chin et al [U.S 6,202,10i], in view of Trieu et al [U.S 6,314,472], and further in view of Nakano et al [PN 6.263.406].

12. As per claim 26:

Chin-Trieu teaches the claimed system as mentioned above.

includes terminating data received from the first memory device, wherein the data is associated with the first request.

Karl teaches terminating first request includes terminating the first request in a memory controller, in response to the first notification, before the first request is sent to the first memory device; terminating first request includes terminating data received from the first memory device, wherein the data is associated with the first request [abstract; col. 1, line 10 to col. 2, line 65].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Karl's teaching into Chin's method of processing data. Doing so would reduce unnecessary requests to memory, wherein a request is no longer need because the latest data were found in the cache. Such excessive requests typically wastes processor resources by tying up the bus interface and other processor resources. The memory controller will not waist extra cycles to process unneeded requests. Furthermore, this provides an opportunity to re-balance requests to the memory controller [Karl, abstract; col. 1, lines 30-65].

2.As per claim 5-7:

Chin further teaches the data in the second memory is coherent with the data in the first memory [col. 3, lines 50-60]; the first memory device is a RAM [col. 2, lines 63-67]; the second memory includes cache memory [16, fig. 1].

3.As per claims 9- 11:

Chin teaches the first request is generated by a client [I/O, 32, fig. 1] on a system bus; the memory request includes a multiple target memory request [16, 18, fig. 1]; and the step of providing a second request includes: providing the second request to a bus interface unit [14, fig. 1], wherein the bus interface unit is coupled to the second memory device [16, fig. 1; col. 2, line 55 to col. 3, line 65].

Claims 12-25, 27 are rejected under 35 U.S.C 103(a) as being unpatentable over Chin et al [U.S 6,202,10], and in view of Trieu et al [U.S 6,314,472].

4.As per claims 12-13, 15:

Chin teaches a method comprising the steps of receiving a first request to read data from a memory device; preparing a second request, based upon the first request, for transmission to the memory device; delivering a third request, based upon the first request, for data from a cache memory, the third request being delivered concurrently with the preparation of the second request [abstract; col. 1, lines 9-15; col. 7, line 20 to col. 8, line 65; col. 11, lines 45-55].

Implicitly, Chin teaches: providing, in response to the first request, data from the cache memory when the data stored in the cache memory is coherent with the data stored in the memory device. This is because request for data can be satisfied and faster from the second memory device [cache] instead of from the comparatively slower regular first memory device [main memory]; providing, in response to the first request, data from the memory device when the data stored in the cache memory is not coherent with the data stored in the memory device. This is because in order to ensure system coherency, a fresh data must be provided to the requestor from other memory device once the system detects a stale/invalid data in a cache memory [col. 3, lines 33-65; col. 4, lines 15-60].

Chin does not teach terminating the second request when the data is provided from the cache memory; a memory controller is used for terminating the second request. Trieu teaches terminating the second request in a memory controller [col. 3, lines 5-65; col. 4, lines 25-65].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Trieu's teaching into Chin's method of processing data. Doing so would reduce unnecessary accesses to memory, wherein a request is no longer need because the latest data were found in the cache. Such excessive requests typically wastes processor resources by tying up the bus interface and other processor resources. The memory controller will not waist extra cycles to process unneeded requests The time otherwise may be used to process unneeded requests by the memory controller may be used to process other requests coming from other system resources [Trieu, col. 1, lines 20-40; col. 5, lines15-20].

5. As per claim 14:

Chin-Trieu does not teach terminating the second request includes further stopping data from the memory device from being provided in response to the first request. However, It would have been obvious that terminating the second request includes further stopping data from the memory device from being provided in response to the first request, because the second request is based upon the first request.

6. As per claim 16:

Chin teaches that the first request is generated by a bus client [32c, fig. 1; col. 8, lines 1-10].

7. As per claims 17-18:

Chin teaches the client is a multiple target memory request. [16, 18, fig. 1], and delivering a third request includes: delivering the third request to a bus interface [14, fig. 1]; and wherein the bus interface unit is coupled to the cache memory [16, fig. 1; col. 2, line 55 to col. 3, line 65].

8. As per claim 19, 27:

Chin teaches a system comprising:

a data processor [12, fig. 1] having: an input/output buffer [30b, fig. 1]; and cache memory [16, fig. 1] to store data associated with a memory device; a bus interface unit [14, fig. 1] having a first input/output buffer coupled to the input/output buffer of the data processor, a second input/output buffer [24, fig. 1] and a third input/output buffer [50a, fig. 2] said bus interface unit to: determine a validity [e.g., coherency] of data in said cache memory during a cache access ; and provide a notification indicating data in said cache memory is valid [col. 3, lines 45-65; col. 4, lines 55-60]; Implicitly, Chin teaches said notification identifies a first request. This is because when the CPU or I/O device generates a plurality of requests, each request must have its own identification so the memory controller can return requested data to appropriate request [col. 3, line 65 to col. 4, line 55];

memory device having an input/output buffer coupled, said memory device to provide data associated with a first request; a bus controller having a first input/output buffer coupled to the input/output buffer of the data processor, a second input/output

buffer coupled to the second input/output buffer of the bus interface unit and a third input/output buffer, said bus controller to:

receive said first request to access data in said memory device, wherein said equest is received from a bus client [16, fig. 1]; provide said first request to the memory controller [44, fig. 2]; receive said data associated with said first request from said bus interface unit [14, fig. 1]; the memory controller having a first input/output buffer coupled to the third input/output buffer of the bus controller, a second input/output buffer coupled to the third input/output buffer of the bus interface unit and a third input/output buffer coupled to the input/output buffer of the memory device, said memory controller to:

provide access to said memory device;

receive said first request from said bus controller [40, fig. 2]; prepare said first request to access data from said memory device; provide a second request to said bus interface unit, wherein said second request is to access data associated with said first request from said cache memory; receive said notification from said bus interface unit [fig. 1-2; col. 7, line 20 to col. col. 9, line 40].

Chin does not teach that terminate the first request, in response to the receipt of notification.

Trieu teaches terminate the first request, in response to the receipt of notification [col. 2, lines 1-65].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Trieu's teaching into Chin's method of processing data. Doing so would reduce unnecessary accesses to memory, wherein a request is no longer need because the latest data were found in the cache. The memory controller will not waist cycles to process unneeded requests. The time otherwise may be used to process unneeded requests by the memory controller may be used to process other requests coming from other system resources [Trieu, col. 1, lines 20-40; col. 5, lines15-20].

Chin-Trieu does not teach storing identifier as part of a kill list, wherein kill list dentifies request to be terminated.

Nakano teaches storing identifier as part of a kill list, wherein kill list identifies request to be terminated [e.g., table delete request].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Nakano 's teaching into Chin-Trieu's computer system. Doing so would increase the deleting request process, because all identifier of requests being deleted are gathered and stored in a table and the memory controller can purge all of these requests at once.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H. Yoo, can be reached on (703) 308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ND

NGOC DINH
Patent Examiner
ART UNIT 2187
April 30, 2003

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100